TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Electrical and Computer Engineering Vodafone Chair Mobile Communications Systems

Vector Processors for Baseband Processing

Bachelor/Master/Diploma Thesis
Studienarbeit/Diplomarbeit

Problem Statement

Vector processors execute a single instruction on multiple data items (SIMD) in a time- and space-division multiplexed (TDM and SDM) manner. This reduces the instruction fetch and decode overhead making vector processors a promising technology for scalable and energy-efficient computing [1]. Popular instruction set architectures (ISA) have added extensions for vector processing, e.g. ARM [2] or RISC-V [3]. Depending on your interests, you can study different hardware (HW) and software (SW) implementation aspects of vector processors for baseband processing and make a comparison between different architectural choices.

Tasks

- Learning about vector processor fundamentals
- Running simulations of open-source RISC-V vector processor implementations [4,5]
- Analysis and written documentation of the results in German or English

Expected Skills

- Working with tools in a Linux command line environment
- For SW: Experience in embedded programming (C and Assembler)
- For HW: Experience in HW design (Verilog or Chisel/Scala)

Contact Person

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Please include a recent transcript of records when contacting.

Recommended References

[1] D. Dabbelt, C. Schmidt, E. Love, H. Mao, S. Karandikar, and K. Asanovic, " Vector Processors for Energy-Efficient Embedded Systems," in *Proceedings of the Third ACM International Workshop on Many-core Embedded Systems (MES '16)*. Association for Computing Machinery, New York, NY, USA, pp. 10–16, 2016, https://doi.org/10.1145/2934495.2934497.

[2] N. Stephens et al., "The ARM Scalable Vector Extension," in IEEE Micro, vol. 37, no. 2, pp. 26-39, Mar.-Apr. 2017, https://doi.org/10.1109/MM.2017.35.

[3] RISC-V Foundation, "Working draft of the proposed RISC-V V vector extension", [Online], https://github.com/riscv/riscv-v-spec.

[4] M. Cavalcante, F. Schuiki, F. Zaruba, M. Schaffner and L. Benini, "Ara: A 1-GHz+ Scalable and Energy-Efficient RISC-V Vector Processor With Multiprecision Floating-Point Support in 22-nm FD-SOI," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 2, pp. 530-543, Feb. 2020, https://doi.org/10.1109/TVLSI.2019.2950087.

[5] Chipyard, "Hwacha", [Online], https://chipyard.readthedocs.io/en/latest/Generators/Hwacha.html.